

# 10-bit 700MS/s SAR-ADC

## Product Brief:

IC4X's **ADC10\_700MS** is a compact, ultra-fast analog-to-digital converter optimized for advanced mixed-signal and RF systems requiring multi-hundred-MS/s performance with deterministic latency. Operating with a clock frequency of up to 9.8 GHz, the SAR-ADC achieves an impressive 700 MS/s conversion rate, enabled by a streamlined architecture featuring 1 clock cycle for sampling followed by 13 conversion cycles.

Digital output data becomes available after 21 clock cycles, providing predictable timing for high-speed digital processing pipelines. The SAR-ADC occupies a highly efficient  $153\mu\text{m} \times 28\mu\text{m}$  footprint, making it ideal for dense SoCs, multi-channel ADC arrays, and next-generation communication ICs.

## Key Features:

### SAR ADC:

- $f_{clk} \leq 9.8\text{GHz} \rightarrow 700\text{MS/s}$  conversion rate
- 1 clock cycles sampling, 13 conversion cycles
- Digital output is available after 21 clock cycles
- Intrinsic 11-bit cap array matching

### ADC area:

- $153\mu\text{m} \times 28\mu\text{m}$  (W x H)

## Technology Requirements:

- Fully Silicon verified
- GF22FDX Metall Stack #19

## Applications:

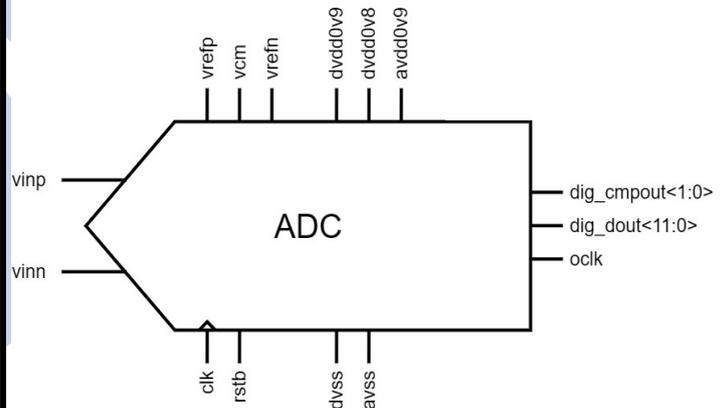
- Wireline, wireless and optical applications
- Highly time-interleaved ADCs

## Contact us!

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IP #: ADC10\_700MS\_ADC

## System Block Diagram:



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## Specifications and Characteristics:

Parameter	Comment	Min.	Typ.	Max.	Unit	Cond.
Bandwidth	3dB input attenuation	>5			GHz	sim
Sampling Frequency, $f_s$		1		700	MS/s	sim
Input Clock, $f_{clk}$			$14 \cdot f_s$			info
ENOB			7.6		bit	sim
SNDR	RCC extracted, $f_s = 700\text{MS/s}$ , Noise on, 256pts, $f_{in}=8\text{MHz}$		48		dB	
SNR			48		dB	
SFDR			62		dBc	
ENOB			7.7		bit	meas.
SNDR	Measured, $f_s = 430\text{MS/s}$ Speed limited by measuring equipment		48		dB	
SNR			48		dB	
SFDR			67		dBc	
Supply			-5%	0.9	+5%	V
Temperature	Junction Temperature	-40	25	125	°C	info
Input Common Mode	DC-Coupled		0.6		V	info
Input Full Scale	Peak-to-peak, differential, $V(vrefp) = 0.9\text{V}$ , $V(vrefn) = 0\text{V}$		1.3		V	sim
Power Consumption	ADC Core		8.5		mW	sim

## Measurements Results:

For the tapeout, an on-chip decimator was added. It resamples the digital output at  $1/8^{\text{th}}$  of the original sampling rate.

