15-60MS/s Frequency-Agile CT ∑-Δ ADC

Product Brief:

IC4Xs' **ADC14_15to60MS_22FDX** is a low-noise, wide-band, continuous-time Σ-Δ ADC converts a fully differential analog input signal into an oversampled 4-bit data stream. The decimator (available on request) delivers 14-bit resolution at 15 to 60MS/s output data rate (for sampling speeds ranging from 0.24GHz to 0.96GHz). The ADC core including the RC calibration engine operates from a 0.9V (±5%) power supply. This way, the ADC is protected against reliability, robustness, and lifetime issues.

The ADC full scale input range is $1.2V_{ppd}$ (max) making it ideal for applications which require a wide dynamic range with high common-mode rejection.

The ADC features a fast inherent overload recovery as well as an external digitally controlled loop-filter reset.

The additional RC time constant calibration engine enables seamless (user-friendly) process, and temperature tracking with 4% (typical) RC calibration step.

This enables beside a fully frequency-agile sampling operation range from 240MHz up to 0.96GHz also a process- and temperature-independent noise-transfer function correction.

Furthermore, manufacturing- and aging-related mismatch effects are mitigated using an in-the-loop data weighted averaging (DWA) block. Hence, excellent linearity in terms of spurious free dynamic range 80 dBc (typical) and total harmonic distortion 75dB (typical) is guaranteed. Spectral purity at reduced ADC input amplitudes is guaranteed by design.

The 800Ohm ADC input impedance remains constant across the entire bandwidth range, relaxing the drive capabilities of the proceeding ADC driver.

The ADC provides an inherent anti-aliasing filter rejection of 70dB (typical) at $f_{clk} \pm f_{Nyq}/2$.

Key Features:

- RC time constant calibration enables frequency agile operation from 0.48 to 0.96GHz input clock frequency
- Input impedance: 800Ω (typical)
- Signal to noise ratio (SNR): 74dB (typical)
- Effective number of bits (ENOB): 11.8-bit
- Dynamic range (DR):
- 12-bit no missing code
- Full scale analog input range: $1.2V_{ppd}$ (max)
- Current Consumption: 33mA (max)
- On-board digital calibration engine
- Operating temperature -40°C to 125°C
  Excellent 2:1 silicon aspect ratio for placement in I/Q receiver applications
- Inherent anti-aliasing filter properties
- CML clock input interface ($600mV_{ppd}$)
- Data Weighted Averaging (DWA) mismatch shaping option
- Δ-∑ modulator core area: $0.4mm^2$
- Silicon proven in 22FDX from GF

Technology Requirements:

Isolation features: S3, BFmode
Metall Stack: 19
S3 and BFmode applied for superior substrate noise isolation.

Applications:

- High-speed data acquisition systems
- Wireless Receiver for LTE, LTE-A, 5G
- Optical networking
- Automotive
- Software defined radio

Contact us!

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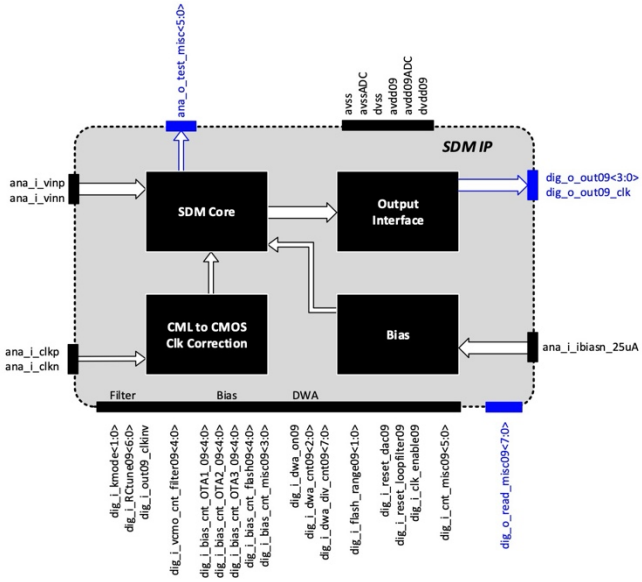
IP #: ADC14_15to60MS_22FDX

System Block Diagram



IC4X INTEGRATED CIRCUITS & SYSTEMS

Specifications and Characteristics Across Entire Bandwidth Range:

T_A = 25°C

Parameter	Min.	Typ.	Max.	Unit	Comments
SNDR	68	72		dB	1-tone 1.5MHz -1dBFS input;
SFDR		80		dBc	1-tone 1.5MHz -1dBFS input
Input range		1	1.2	V_{ppd}	
Power Supply	-5%	0.9	+5%	V	
RC time constant calibration		4%	7%		
f_{clk}	0.48		0.96	GHz	Input clock
Input Impedance	-25%	800	+25%	Ω	
Output Interface		4		bit	Binary; w/o decimator
Power Consumption			30	mW	Modulator only (digital and analog)

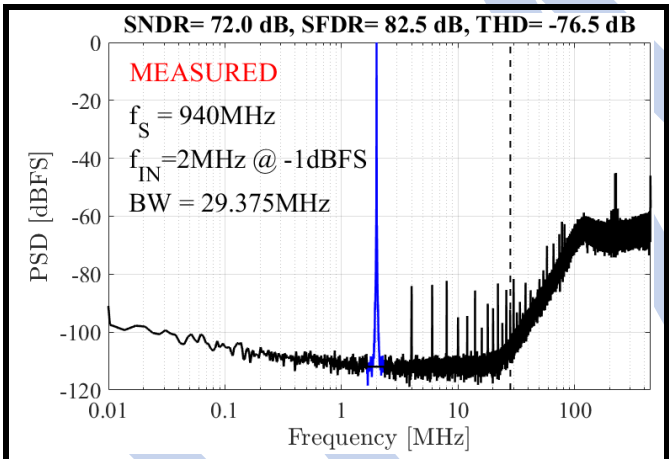
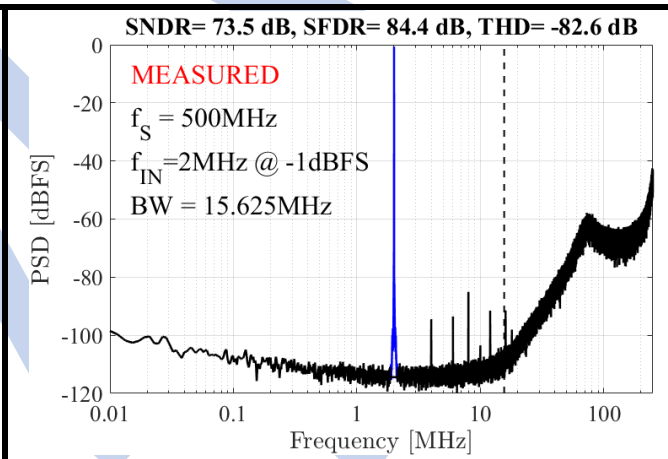


Fig. 1:~Spectral Performance @ 60MS/s



Spectral Performance @ 30MS/s

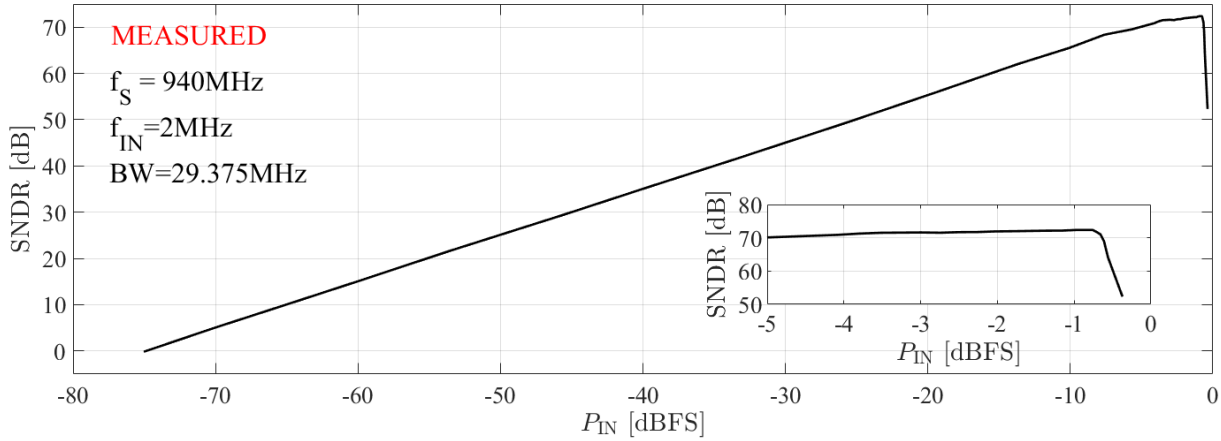


Fig. 3:~ SNDR across P_{IN} @ 60MS/s